What is claimed is:

[Claim 1] 1. A method for developing a design of an integrated circuit, said method comprising steps of:

selecting a smallest chip image from among a plurality of chip images that can supply at least a required number of I/O cells;

determining a number of excess I/O kernels of said smallest chip image in excess of said required number of I/O cells;

computing a number of other cells types which can be provided by the core area of the image and the area of the excess I/O kernels; and

evaluating from a result of said computing step if a required number of cells for said integrated circuit design can be provided within said smallest chip image if said excess I/O cells or I/O kernels are depopulated from said smallest chip image.

[Claim 2] 2. A method as recited in claim 1, wherein, if the required number of cells for said integrated circuit design can not be provided, said method includes the further step of selecting a next larger chip size and repeating said determining computing and evaluating steps.

[Claim 3] 3. A method as recited in claim 1, including the further step of selecting a smallest package size providing said required number of I/O cells and said step of selecting a smallest chip image is performed by selection from chip images corresponding to said smallest package size.

[Claim 4] 4. A method as recited in claim 2, including the further step of selecting a smallest package size providing said required number of I/O cells and said step of selecting a smallest chip image is performed by selection from chip images corresponding to said smallest package size.

[Claim 5] 5. A method as recited in claim 4, including the further step of determining, when a said larger chip size can provide said required number of cells, performing the further step of:

determining if said larger chip size can be accommodated by said package and, if not, selecting a larger package size.

[Claim 6] 6. An integrated circuit including:

an array of I/O kernels, each I/O kernel having a plurality of contiguous I/O cells having common power connections, independent of any other I/O kernel; and

a plurality of contiguous depopulated I/O cell sites corresponding to an area of a said I/O kernel and having core cells formed therein.

[Claim 7] 7. An integrated circuit as recited in claim 6, further including some off-chip connection pads corresponding to the said depopulated I/O kernel.

[Claim 8] 8. An integrated circuit as recited in claim 7, further including all off-chip connection pads corresponding to the said depopulated I/O kernel.

[Claim 9] 9. An integrated circuit as recited in claim 6, wherein said I/O kernels are arranged with substantially radial symmetry along edges of a semiconductor chip.

[Claim 10] 10. An integrated circuit as recited in claim 6, wherein said plurality of contiguous depopulated I/O cell sites corresponding to an area of a said I/O kernel include a corner kernel.

[Claim 11] 11. An integrated circuit as recited in claim 6, wherein said plurality of contiguous depopulated I/O cell sites corresponding to an area of a said I/O kernel include an edge kernel.

[Claim 12] 12. An integrated circuit as recited in claim 6, including at least two pluralities of contiguous depopulated I/O cell sites corresponding to an area of a said I/O kernel on a single edge of a chip, said two pluralities of contiguous depopulated I/O cell sites being separated by an I/O kernel.

[Claim 13] 13. An integrated circuit as recited in claim 6, further including:

a metal power connection through a said depopulated I/O cell site.

[Claim 14] 14. An integrated circuit having peripheral connections pads including:

I/O cells associated with a contiguous plurality of said connection pads and a plurality of contiguous depopulated I/O cell sites associated with a contiguous plurality of other of said connection pads; and

power connections to said other connection pads and logic cells located in said depopulated I/O cell sites.